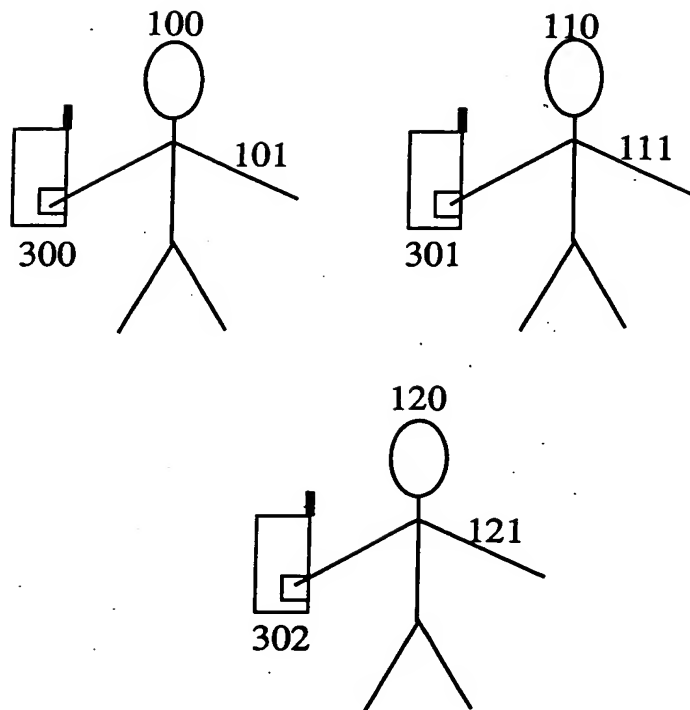


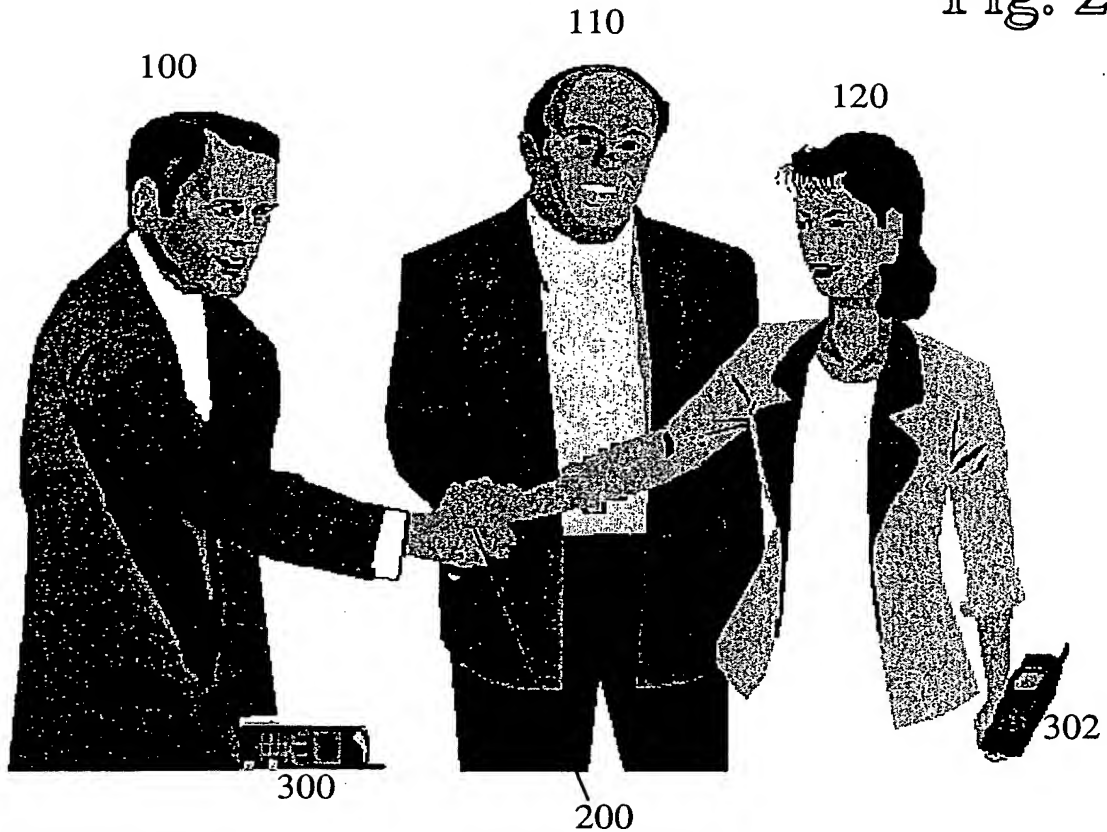
Fig. 1



10027501.041502

BEST AVAILABLE COPY

Fig. 2



10027501.041502

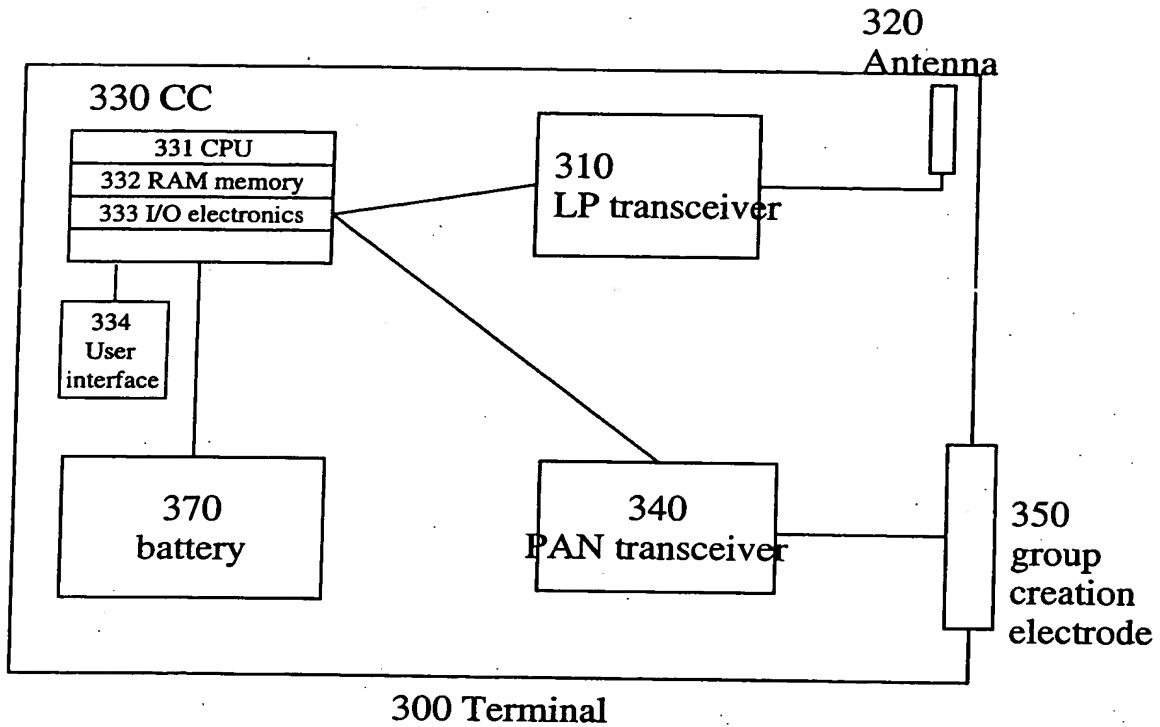


Fig. 3

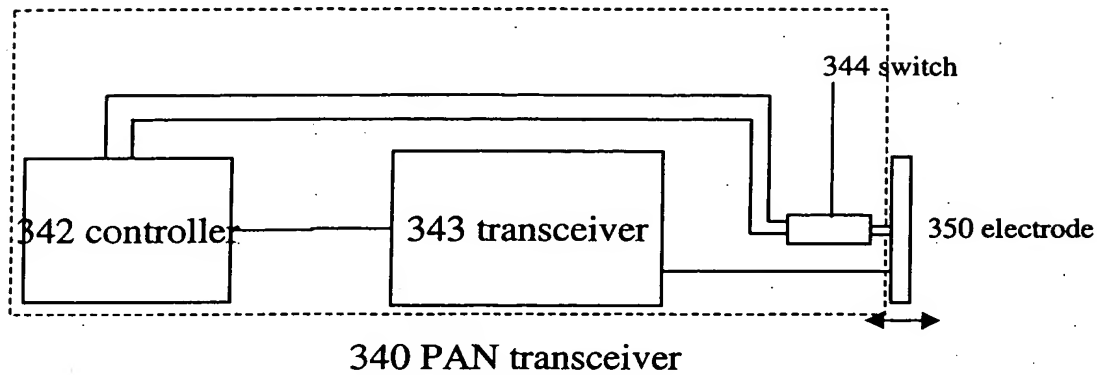


Fig. 4A

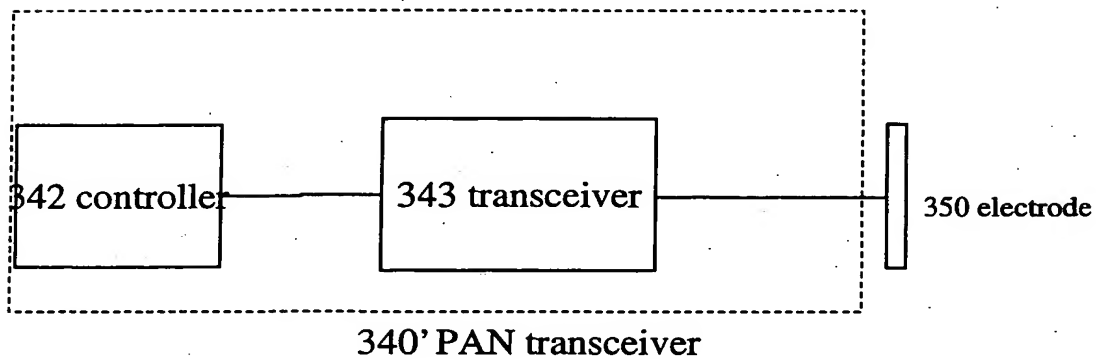


Fig. 4B

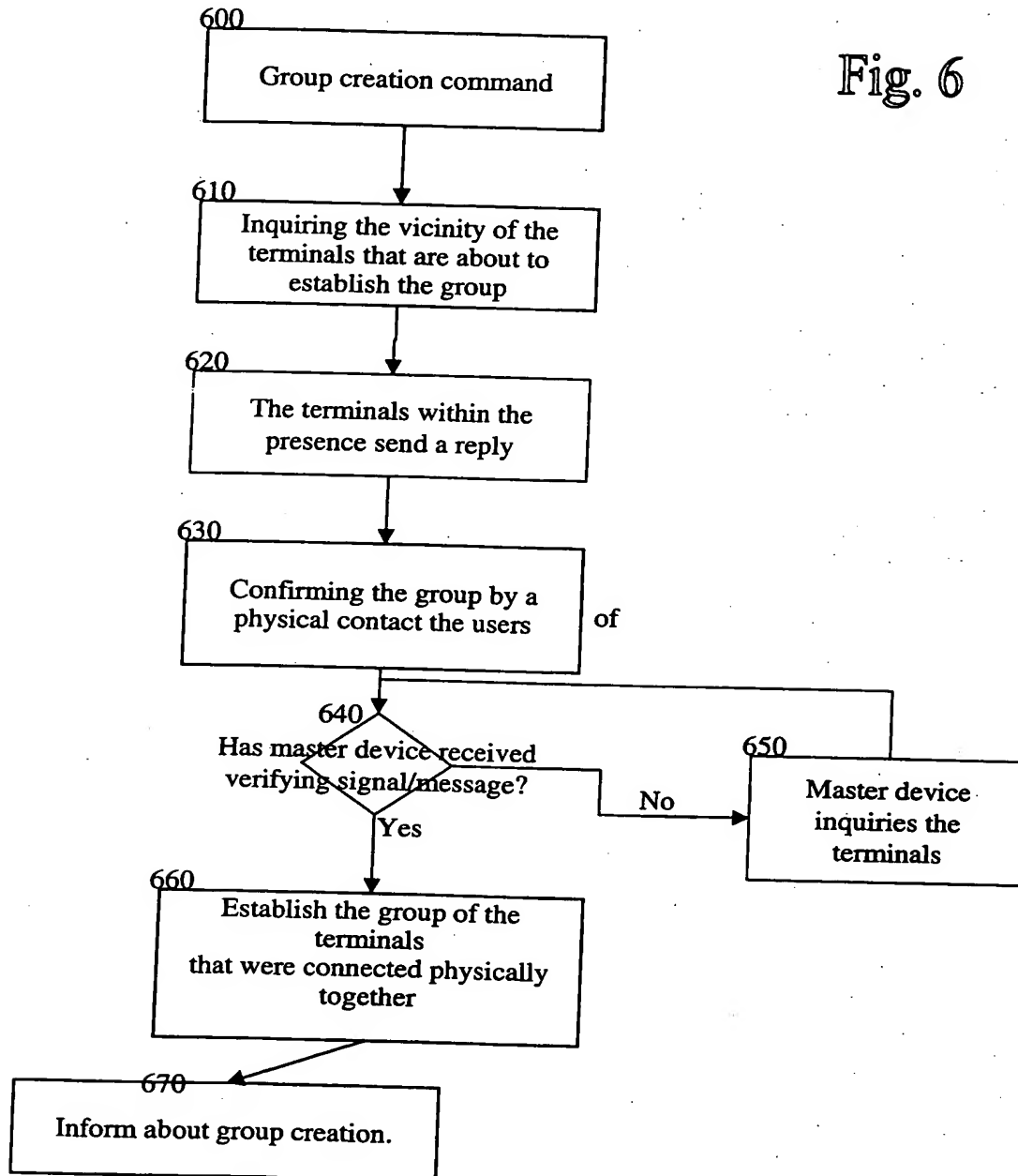
10027501.04.1502

501	502	503	
BD_ADDR	Clock Offset	Class of Device	

Fig. 5

10027501.011502

Fig. 6



10027501.01.1.002

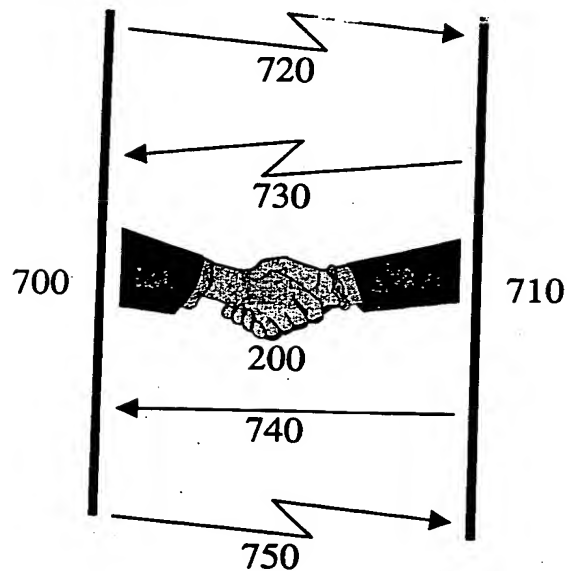


Fig. 7

10027501.041502

Fig. 8

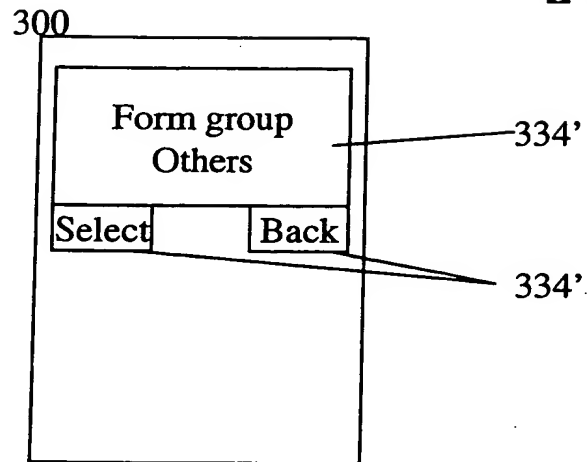
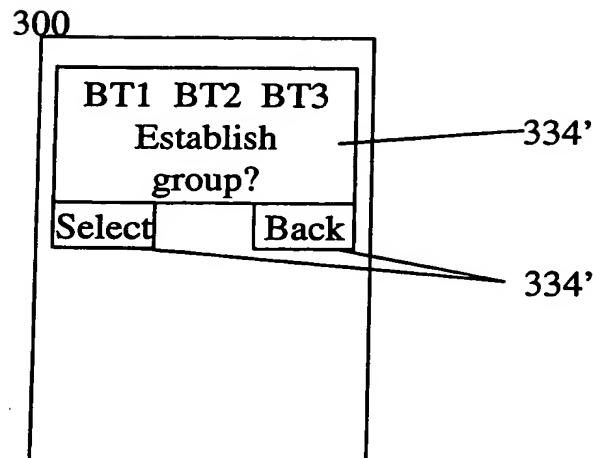


Fig. 9



10027501.011502